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Electrical characterization of a-Si:H(n)/c-Si(p) structure

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ABSTRACT

In this study, n-type hydrogenated amorphous silicon (a-Si:H) was fabricated on p-type crystalline silicon (c-Si) substrates to obtain heterojunction diodes. The amorphous films were obtained by the Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. Temperature dependent current–voltage (*I–V–T*) measurements and investigation of the dc current injection mechanism of a-Si:H(n)/c-Si(p) device structure have been performed. The series resistance (4.6–8.2 Ω) values displayed nearly temperature independent behavior and the ideality factor varied between 2.7 and 1.6 in the temperature range 100–320 K. The forward bias *I–V–T* characteristics of c-Si/a-Si:H heterojunctions are found to behave like the Schottky junctions where carrier injection is especially influenced by the carrier generation-recombination in the junction interface formed on the amorphous side. The temperature dependent ideality factor behavior shows that tunneling enhanced recombination is valid rather than thermionic emission theory. In the frame of this model, characteristic tunneling energy and characteristic temperature are found to be 9 meV and 1900 K, respectively. It is concluded that fabricate n-type hydrogenated amorphous silicon is a preferable semiconductor material layer with low interface state density because the temperature dependent interface state density calculations give values of the order of 10^{14} eV^{-1} cm^{-2}.

1. Introduction

Solid state device physics is the branch of science that deals with electronically circuits involving active electronic components such as diodes and transistors. The diodes are one of most important and smallest cell in the electronic circuitry. The nonlinear behavior of these components and their ability to control electron flows make rectification of any signals or amplification of weak signals possible, and is usually applied to information and signal processing. Today, most diodes such as Schottky barrier diodes, heterojunction diodes and metal–insulator–semiconductor (MIS) diodes use semiconductor materials to perform electron control. Reducing the cost of the diode fabrication remains one of the most important issues in the electronic chip industry. Due to the abundance of raw silicon material in nature, its favorable electrical and physical semiconductor properties and the ability to produce large scale wafers for the fabrication of devices and circuits, silicon has become the material of choice in the electronics industry. However, fabrication cost of crystal silicon is not cheap. To overcome the high fabrication cost of crystal silicon, one can propose a-Si:H as an alternative material due to low cost production [1]. a-Si:H materials are received as popular semiconductors with electronic properties and they have attained an extensive application area in electronic technology. N-type a-Si:H has been admitted as one of the candidates for several optoelectronic applications such as position sensitive sensors [1–3] and diode because of its good environmental stability, easy conductivity control and cheap production in large quantities [1]. The subsidence and understanding the role of Staebler Wronski (SW) effect have induced a number of studies on a-Si:H and it has been widely studied due to its technologically considerable applications. It is much more flexible in its applications. For example, a-Si:H layers can be made thinner than c-Si, which may produce savings on silicon material cost [1]. In that point, a-Si:H is a quite attractive and good candidate as a p-type and n-type layer. a-Si:H semiconductor can be deposited over large areas by PECVD system. The design of the PECVD system has big effect on

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the actual cost and quality of such a semiconductor material, hence research instrument manufacturers tend to focus on the design of PECVD for higher throughout, that leads to lower manufacturing cost [1,3].

a-Si:H has become the material of choice for the active layer in thin-film transistors (TFTs), which are most widely used in large-area electronics applications, mainly for liquid–crystal displays (LCDs). Recently, heterojunction devices, which include a-Si:H material as an active layer, have become very popular to provide tunable operating voltage for low power devices due to easy fabrication process as a very thin layer [1–9].

The electronic properties of a-Si:H material and its interfaces have an active part in determining the performances of MIS devices based on Schottky barrier structures. Ascertaining the diode properties and electrical conduction mechanisms in these devices are fundamental step in the task of improving device performance. There have been substantial experimental researches on the metal–semiconductor (MS) and metal–insulator–semiconductor (MIS) type Schottky barrier diodes (SBDs) [10–12].

The importance of such studies is to understand the effect of native or deposited insulator layers in MIS type SBDs [10–20]. The formation of device structure strongly effects to the performance and stability of these devices [9]. In spite of these numerous studies, more work is needed to understand the fundamental characteristics of a-Si:H/c-Si heterojunction diode structures and the key factors required to improve their electronic quality. On the other hand, the interface properties between n- and p-type materials are crucial [1–20].

A few experimental studies have been performed to display the effect of a-Si:H material as a n-type layer in device application [1–9]. However, the temperature (T) dependent dark I–V characteristics of c-Si/a-Si:H device structure are still unknown. For that reason, detailed investigation of the electrical characteristics is required to extract the temperature dependent barrier height (BH) and ideality factors from the measured non-ideal I–V data in the presence of a hydrogenated amorphous silicon (a-Si:H). In this article, we have investigated the dark forward bias I–V characteristics of c-Si/a-Si:H device in the temperature range of 100–320 K. The forward bias I–V–T measurements are used to explain the current transport mechanism and to estimate the device parameters. Also, the temperature dependent interface BH of c-Si/a-Si:H device is interpreted based on the existence of the interface state prevailing at the semiconductor/amorphous layer interface.

2. Experimental procedures

a-Si:H/c-Si heterojunctions were deposited on the top of ⟨1 0 0⟩ oriented, 3″ diameter, 1–10 Ω cm resistivity, and p-type boron doped Czochralski silicon wafers. After RCA cleaning, ohmic aluminium electrodes were formed on the back surface.Heterojunctions were deposited in a commercial multichamber UHV PECVD system (M.V. Systems). Plasma excitation frequency was 13.56 MHz, the rf power density was ~40 mW/cm^2, chamber pressure was 0.7 Torr, substrate temperature was 300 °C and deposition duration was 5 min. Reactant gases were 1% PH_3 in H_2 and pure SiH_4. Doping concentration was fixed at 2.5×10^{-4} ($[PH_3]/[SiH_4]$) and was controlled using MKS System Mass Flow Controllers.Thickness of deposited n-doped a-Si:H films were determined from spectroscopic elllipsometry measurements (Jobin Yvon – UVISEL) and found to be 50–80 nm. After deposition the Al grid contacts with two 1.5 mm width bus bars and fingers were evaporated on the front side of the solar cells. The structure of c-Si/a-Si:H device is given in Fig. 1.

Measurement was performed inside an evacuated OXFORD cryostats. The device was connected to Keithley 236 Source/Measure unit for dc measurement via equipped suitable coaxial cable. Measurement was automated with a personal computer. A delay of a few seconds between subsequent measuring steps was built into the program to assure steady-state conditions for the measurement of the current. In addition, for each voltage step, the average of up to 32 current measurements were taken to increase the signal-to-noise ratio and extend the range of current measurement down to 2×10^{-14} A.

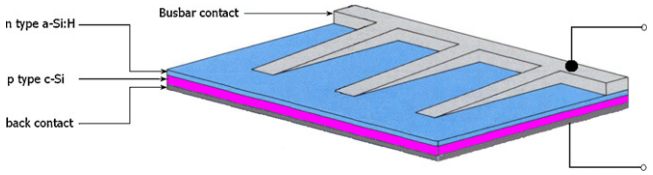

Fig. 1. Schematic diagram of p-Si/a-Si:H structure.

3. Results and discussion

The a-Si:H/c-Si structure behaves like a Schottky barrier diode [5,8,9]. Thermionic emission (TE) theory predicts that the current–voltage characteristic is given as follows [10–12,22–29]:

$$I = I_o e^{(q(V-IR_s))/(nk_BT)}[1 - e^{-(q(V-IR_s))/(k_BT)}] \quad (1)$$

where I is the measured current, V the applied voltage, R_s the series resistance, q the electronic charge, k_B the Boltzmann constant, T the absolute temperature in Kelvin, n the ideality factor that describes departure from the ideal diode equation for reverse bias as well as forward bias. I_o is the reverse saturation current derived from the straight-line intercept of $\ln I$ at zero bias and is given by

$$I_o = AA^*T^2 e^{-(q\Phi_{B0})/(k_BT)} \quad (2)$$

where A is the device contact area, A^* the effective Richardson constant, equal to 32 A cm^{-2} K^{-2} for p-type Si, and Φ_{B0} the BH at zero bias, which can be calculated from Eq. (3):

$$\Phi_{B0} = \frac{k_BT}{q} \ln\left(\frac{AA^*T^2}{I_o}\right) \quad (3)$$

n values are calculated using I–V curves given in Fig. 6, according to TE theory. Using Eq. (1), the value of n is derived as

$$n = \frac{q}{k_BT}\left[\frac{dV}{d(\ln I)} - IR_s\right] \quad (4)$$

Under moderately forward-bias condition ($(k_BT/q) > V > 0.4$ V), voltage across the series resistance (IR_s) can be neglected. Then, Eq. (4) is simplified to equation (5):

$$n = \frac{q}{k_BT}\frac{dV}{d(\ln I)} \quad (5)$$

The value of n is inferred from the slope of the linear region of the forward-bias $\ln I$–V plot by using Eq. (5).

I–V characteristics of the c-Si/a-Si:H device measured at various temperatures ranging from 100 to 320 K are given in Fig. 2. As can be seen in this figure, I–V curves are linear on a semi-logarithmic scale at the moderately forward-bias voltage region, but they depart significantly from linearity at high forward-bias voltages due to the effects of some factors such as series resistance, interfacial layer and interface states. The series resistance has an influence on the forward bias I–V characteristics at the high injection region ($1.4 \leq V \leq 2$).

R_s was calculated from the data belong to I–V curve is not linear (in the high current range) using a method developed by Cheung and Cheung [30]. According to this method, Eq. (4) can be rewritten as

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{k_BT}{q}\right) \quad (6)$$

The plot of $dV/d(\ln I)$ versus I (Fig. 3) will give R_s as the slope. R_s values vary between 4.6 Ω and 8.2 Ω in the temperature range of 100–320 K. The figure inserted in Fig. 3 shows that the obtained R_s values display nearly temperature independent behavior.

Calculated BH versus ideality factor plot is given in Fig. 4. There is a linear relationship between the experimental zero-bias BH and the ideality factors of the investigated device. The fit to

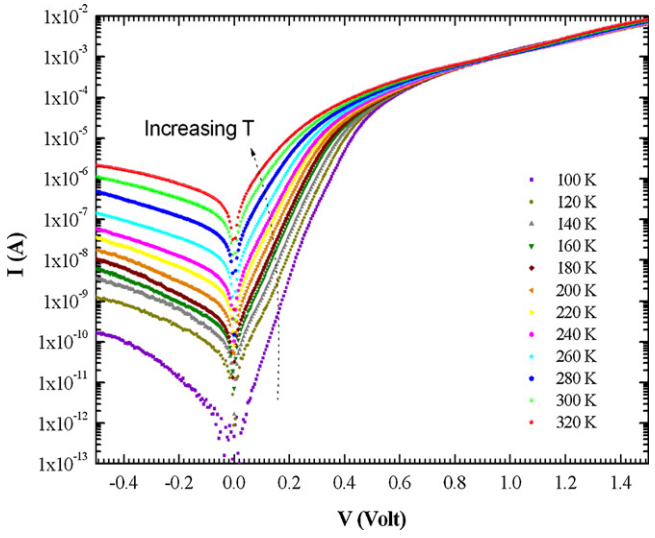

Fig. 2. The experimental forward bias *I–V* characteristics of c-Si/a-Si:H device as a function of temperature.

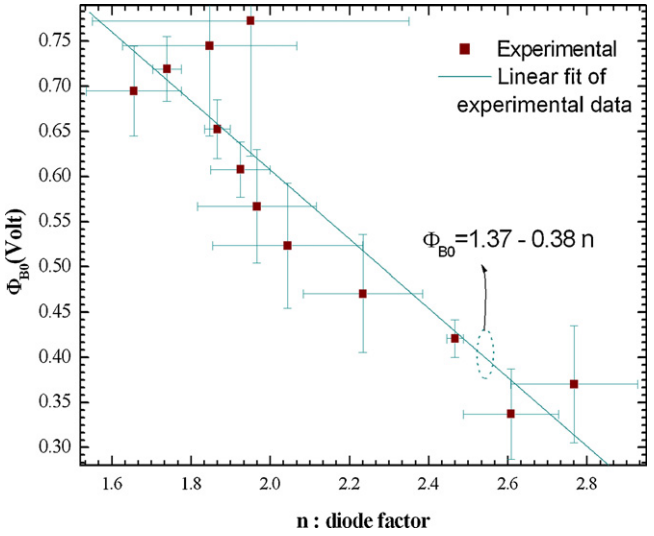

Fig. 4. Linear variation of BH versus ideality factors at various temperatures.

experimental data is performed using least-squares method. Linear relationship between zero-bias BH and the ideality factors can be ascribed to lateral inhomogeneities of the BH in the investigated device [10–12,22–29].

Recently, the effect of the thin interfacial layer in the MS contacts on the barrier modification and ideality properties have been studied experimentally [31–38]. The ideality factor value greater than unity may has originated from the interface states in equilibrium with the semiconductor, interface dipoles due to interface doping or specific interface structure as well as fabrication-induced defects at the interface.

The relation between Φ_{B0} and ideality factor is seen in Fig. 4. Using this relation, homogeneous BH value is calculated as 0.99 eV for $n = 1$. Φ_{B0} and n values in Fig. 4 rigorously stem from the BH inhomogeneities.

The Richardson plot of the device is performed by using Eq. (2). As seen in Fig. 5, there is a linear relation between $\ln(I_o/T^2)$ and $1/T$. The Richardson constant (A^*) has been calculated as 4.33×10^{-10} A cm^{-2} K^{-2} in the temperature range of 100–320 K. This obtained value is much lower than the known value of 32 A cm^{-2} K^{-2} for the p-type Si. These discrepancies are still under debate in the scientific community, and they were attributed to different factors in the publication record [39–43]. Song and Jürgen proposed that spatially inhomogeneous barrier heights and potential fluctuations at the interface could be responsible about such a discrepancy [39,40]. In 1996 Horwath et al. suggested that a value of the real effective mass that is different from the accepted one, automatically leads to observe a lower value of Richardson constant [41]. In additionally, lateral inhomogeneity may cause to observe a lower value of Richardson constant. In a similar way, Tung asserted that observed such a lower value of Richardson constant was not only caused by lateral inhomogeneity but also spatially inhomogeneous BH and potential fluctuation at the interface that consists of low and high barrier regions may cause this observation [42]. However, lately the Roccaforte et al. suggested that an effective device area lower than the geometric area of the device is responsible for the commonly observed discrepancy in the experimental values of Richardson constant from its theoretical value in their device structure. Finally, they concluded that this idea is an eventual physical reason because the quality of device junction's interface is shaped in the device fabrication process [43]. Recently, Janardhanam et al. has studied about Richardson constant

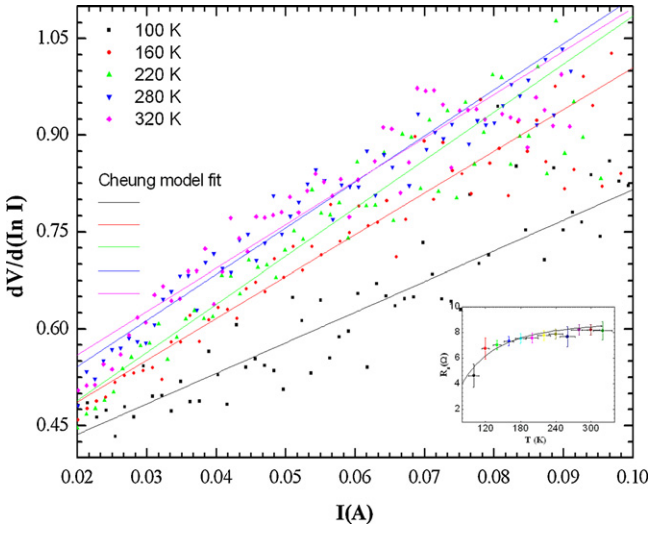

Fig. 3. Plots of $dV/d(\ln I)$ versus I of the c-Si/a-Si:H device.

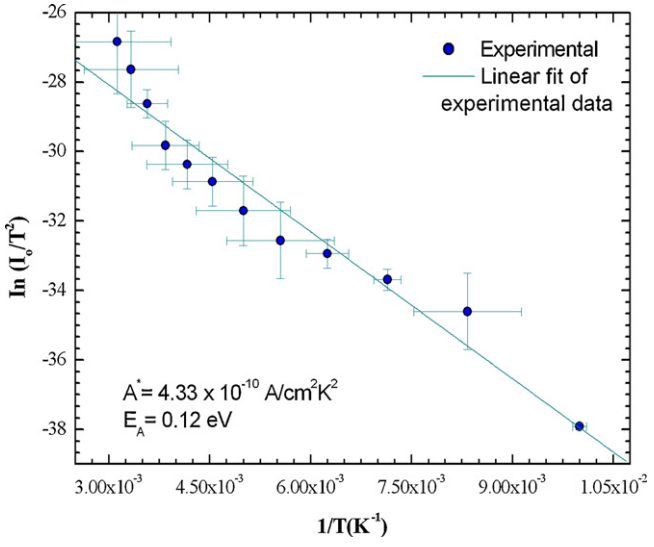

Fig. 5. Regular Richardson plot of the saturation current.

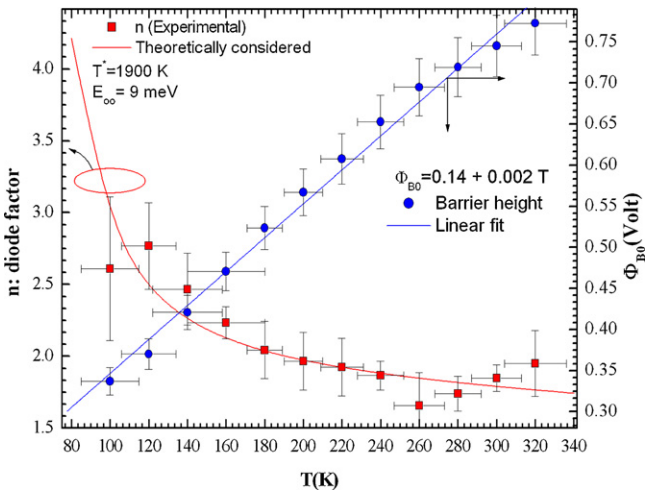

Fig. 6. Temperature dependence of zero-bias BH and ideality factor versus temperature for the c-Si/a-Si:H structure.

of molybdenum Schottky contacts on n-InP. They have reported that the Richardson constant of Schottky diodes does not fit very well with exact value of n-InP. Janardhanam et al. have shown that the spatially inhomogeneous barrier heights and potential fluctuations at the interface that consists of low and high barrier areas is responsible for observation of such a low Richardson constant [44].

In our study, the obtained liner fit from the Arrhenius plot exhibits well-defined linear dependent behavior. As seen in Fig. 5 experimental data point do not exhibit any significant deviation from the linear curve. However, obtained experimental value of the Richardson constant is significantly lower (even orders of magnitude) than the theoretical value of 32 A cm^{-2} K^{-2}. In light of the above discussion, we thought that lateral inhomogeneities of the barrier, spatially inhomogeneous BH and potential fluctuation at the interface may cause such a discrepancy.

Activation energy value has been extracted as 0.12 eV from the slope of the linear fit to the experimental data.

In order to betray the presence of BH inhomogeneity, the temperature dependent ideality factor plot can be examined [13–20,29,31–36]. The ideality factor values are calculated from the slope of forward *I–V* data in Fig. 2. As seen in Fig. 6, ideality factor values increase with decreasing T and lies between 1.60 and 2.75 for T = 320–100 K. n becomes larger than 2 for T < 200 K. These values of n propose that the forward current flows are principally due to carrier generation recombination in the depletion region. However, there are several other publication which also describes the temperature dependence of ideality factor as T_o anomaly [22,40].

The high value ideality factor is a piece of evidence of deviation from the TE theory for the current mechanism. The increase in the ideality factor with decreasing temperature at low temperature region is known as the tunneling effect [10–12,22,40,42]. If the current transport is controlled by the tunneling enhanced recombination (TER) theory due to the SCR (space charge recombination) recombination involves defect states, which can also yield a local reduction of the BH. The relationship between the ideality factor and temperature can be expressed by [21,22,40]

$$n = \frac{2}{1 + (T/T^*) - (E_{oo}^2/(3(k_BT)^2))} \tag{7}$$

where T^* and E_{oo} are constant which are independent of temperature and voltage. This equation represents the diode factor in the case of TER of electron hole pairs via an exponential distribution of recombination centers. Where T^* is the characteristic temperature (characteristic energy corresponds to k_BT^*) of an exponential distribution of recombination centers $N_T(E) \sim \exp(-E/k_BT^*)$. The characteristic tunneling energy (E_{oo}) is independent of temperature. Depending on conditions of experiment, one of them plays a prevailing role [21].

The validity of above Eq. (7) is restricted to a range of $k_BT^* > k_BT \geq E_{oo}$. It is interesting to stress that the diode factor in Eq. (7) becomes equal to $n^{-1} = (1 + T//T^*)/2$ for negligible tunneling contribution. In the limit ($T^* \to \infty$) one obtains a parameter equation which considers for TER via midgap states, while in the limit $E_{oo} \to 0$, one finds $n^{-1} = (1 + T//T^*)/2$ for the picture of typical T^* anomaly effect by way of spatial distribution of trap states. This trap distribution automatically leads to classical SRH (Shockley-Read-Hall) recombination via an exponential distribution of trap states [21]. The variation of n with temperature is demonstrated in Fig. 6. The solid curve in Fig. 6 was plotted by fitting Eq. (7) to the experimental temperature dependent values of the ideality factor. The open squares in Fig. 6 show the temperature dependent values of the ideality factor extracted from the experimental current–voltage characteristics in Fig. 2.

The value of T^* and E_{oo} for the c-Si/a-Si:H device has been found to be 1900 K and 9 meV, respectively in the temperature range of 100–320 K from the functional fit to the experimental data (Fig. 6).

Fig. 6 also shows temperature dependent zero-bias BH behavior. BH increases with increasing temperature as displayed in Fig. 6. Song and Werner [39,40] interpreted this type of behavior as the lateral inhomogeneities of the BH.

The density distribution of the interface states in equilibrium with the semiconductor is extracted by using the forward-bias *I–V* characteristics at each temperature. The ideality factor n can be extracted using Eq. (8) as

$$n(V) = \frac{q}{k_BT}\frac{(V - IR_s)}{\ln(I/I_0)} \tag{8}$$

The presence of an interfacial layer and the interface states located between interfacial layer and semiconductor lead one to assume effective BH (Φ_e) is bias dependent and is given by [10–12,22–28,39–44]

$$\Phi_e = \Phi_{B0} + \beta(V - IR_s) \tag{9}$$

Here β is given by $\beta = 1 - [1/n(V)]$.

The energy of interface states (E_{ss}) with respect to the top of the valence band E_v in a p-type semiconductor is given by

$$E_{ss} - E_v = -q[\Phi_e - (V - IR_s)] \tag{10}$$

If the investigated device structure has interface states in equilibrium with the semiconductor, the ideality factor n becomes greater than unity and can be expressed as

$$n(V) = 1 + \frac{\delta}{\epsilon_i}\left[\frac{\epsilon_s}{W_D} + qN_{ss}(V)\right] \tag{11}$$

where N_{ss} is the density of the interface states in equilibrium with the semiconductor. Eq. (11) for N_{ss} as deduced by Card and Rhoderick [26] is reduced to

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\epsilon_i}{\delta}(n(V) - 1) - \frac{\epsilon_s}{W_D}\right] \tag{12}$$

where ϵ_s and ϵ_i are the permittivities of the semiconductor and the interfacial layer, respectively. δ is the thickness of the interfacial layer, W_D is the width of the depletion region. For each temperature, the values of N_{ss} were calculated from Eq. (12) by substituting δ = 10 Å, $\epsilon_i = 3.8\epsilon_O$ and $\epsilon_s = 11.8\epsilon_O$. The thickness of the interfacial layer was calculated from the capacitance measurements (1 MHz) and was found to be about 10 Å, and this can usually make the values of the ideality factor greater than unity.

Interface state density values vary between 10^{14} eV^{-1} cm^{-2} and 10^{13} eV^{-1} cm^{-2} as seen in Fig. 7. These values are ade-

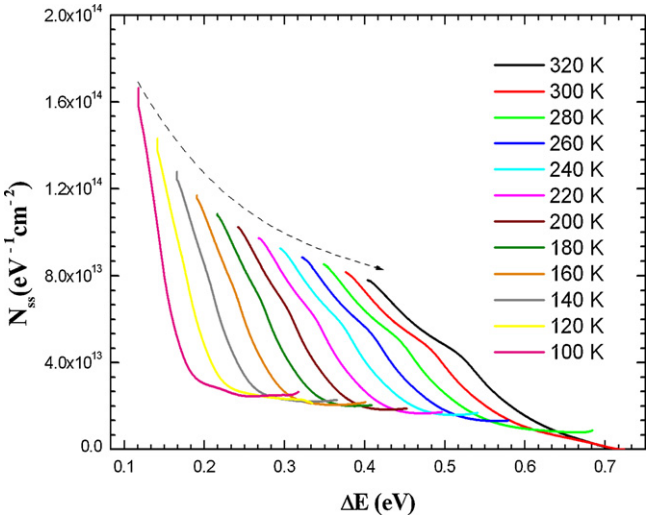

Fig. 7. Density of interface states N_{ss} as a function of ΔE ($E_{ss} - E_v$) deduced from the *I–V* data at various temperatures for the studied c-Si/a-Si:H device.

quately low for each temperature. Interface state density increases exponentially from midgap towards the top of the valence band for all measurement temperatures. These characteristic exponentials trend systematically shift towards higher energy with increasing temperature. MS-type devices with low interface state density are desired and demanded. Thus, one can conclude that fabricated a-Si:H/c-Si devices are favorable candidate of MS-type device applications.

4. Conclusion

- The forward-bias dark *I–V* characteristics of the c-Si/a-Si:H device were measured in the temperature range of 100–320 K.
- n, R_s and Φ_{B0} parameters are calculated using measured dark *I–V* data at all measurement temperatures. The series resistance value displayed nearly temperature independent behavior and the ideality factor varied between 2.7 and 1.6 in the temperature range 100–320 K.
- While Φ_{B0} increases, the ideality factor decreases with increasing temperature.
- Linear relationship between zero-bias BH and temperature has been observed. This observation can be ascribed to lateral inhomogeneities of the BH in the investigated device.
- The experimental values of the ideality factor are in good agreement with the theoretical curve, which is obtained using the characteristic tunneling energy value of 9 meV and characteristic temperature value of 1900 K.
- We have claimed that the domination of TER because the diode factor dominated by negligible tunneling ($E_{oo} \approx 9$ meV).
- The temperature dependent energy distribution of N_{ss} profiles are computed using forward bias *I–V* data. N_{ss} values increase exponentially from midgap towards the top of the valence band for all measurement temperatures.
- We have also observed characteristic tail-like distribution of surface state behavior in our N_{ss} values. A characteristic tail-like distribution is shifted towards the valence band in the N_{ss} plots with increasing temperature. Gap states in n type a-Si:H can be responsible from tail-like distribution, originating from weak Si–Si bonds, or deep states originating mainly from dangling bonds (DB). Due to the inherent disorder of the amorphous lattice, DB can be created at various energy levels, which can lead such a N_{ss} distribution.

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